REMARKS

Reconsideration and allowance of the above-identified Application in view of the above amendments and the following remarks are respectfully requested.

Claim 1 is amended to include the language of claims 2 and 12. Claim 2 is amended accordingly to recite alternate material as disclosed at, e.g. paragraph [0040] of the specification as filed. Claim 12 is amended accordingly to recite alternate material as disclosed at, e.g. paragraph [0038] of the specification as filed. Claims 8–11, 18, and 21 are amended in conformance to claim 1.

Claim 27 is amended to include the language of claim 12 and some of the language of claim 28. Claims 28, 30, and 33 are amended accordingly.

Claim 36 is amended to incorporate acts of determining and altering.

Claim 38 is amended to include the language of claim 44 and some of the language of claim 39, to recite a determination of a logic circuit, and to broaden claim language. Claims 39–43 are amended accordingly, and claim 44 is amended to recite alternate material as disclosed at, e.g. paragraph [0038] of the specification as filed.

Claims 1–44 are pending in the Application.

Rejection under 35 U.S.C. § 103

Claims 1–44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Duluk (U.S. Patent No. 6,476,807). For at least the following reasons, applicant respectfully requests that this rejection be withdrawn.

Claim 1 recites determining that a scratchpad contains an entry mapped to a pixel. Claim 27 recites determining whether a scratchpad contains an entry mapped to a pixel. These claims also recite comparing a Z value of a fragment to a value of the entry, and based on a result of the comparing, passing the fragment to a pixel pipeline.

The Office Action states that Duluk discloses such determining at lines 46–67 of column 20. Applicant respectfully notes that in these lines, Duluk simply describes a particular division

of a window into smaller areas (ll. 46–56; see also FIG. 13A) and "conventional Z buffer rendering" (ll. 61–67). No act of determining whether a scratchpad contains an entry mapped to a particular pixel is disclosed or suggested.

In contrast to the determining recited in applicant's claims, Duluk teaches processing on a tile-by-tile basis, for example in the following portions of column 26:

lines 26–28 (Sort block 6000 sorts vertex information by tile);

lines 39–43 (Sort block 6000 sends sorted output in tile-by-tile order);

lines 47–50 (Setup block 8000 processes data one tile at a time); and

lines 61–62 (Cull block 9000 accepts data one tile at a time).

Applicant respectfully points out that Duluk does not teach determining whether any entry in a tile is mapped to a particular pixel. On the contrary, Duluk teaches away from such a determination – Duluk teaches that a tile corresponds to a (16 x 16) block of pixels (see col. 20, ll. 46–48), such that a correspondence between every entry in the tile and every pixel in the block would already be known and would not change. Consequently, Duluk neither teaches nor suggests an act of determining that a scratchpad contains an entry mapped to a pixel as recited in claim 1, or an act of determining whether a scratchpad contains an entry mapped to a pixel as recited in claim 27.

Claim 12 further recites querying the scratchpad with a location value of the fragment. In reviewing the Duluk reference, applicant has found that the reference teaches "querying" a content-addressable memory MCCAM (col. 30, ll. 35–37). Such a "query" is defined by Duluk as a parallel search comparison operation (col. 13, ll. 11–12). Specifically, Duluk teaches using the MCCAM to perform a comparison, in parallel, between a Z value for a primitive and Z values for every stamp in the current tile (col. 36, ll. 19–31). This teaching of a parallel Z comparison of all values in a tile does not disclose determining that (whether) a scratchpad contains an entry mapped to a pixel as recited in claim 1 (27).

The Examiner notes that Duluk mentions "visible samples" (col. 20, ll. 58–59). Duluk teaches that the MCCAM outputs a list of potentially visible stamps (col. 30, ll. 41–44; FIG. 17). Stamps in this list that are actually touched by the primitive are sent, one at a time, to a Z Cull block 9012 (col. 30, ll. 44–51; FIGs. 13B,C and 18). Duluk teaches that the Z Cull unit 9012

contains a Sample Z Buffer 9055 that **stores all the data for each sample in a tile** (col. 37, ll. 61–65). Because all of the data for the tile is stored, Duluk cannot be said to suggest an act of determining whether data corresponding to a particular pixel is present. Therefore, this teaching of processing of visible samples also does not disclose or suggest determining that (whether) a scratchpad contains an entry mapped to a pixel as recited in claim 1 (27).

For at least the reasons above, applicant respectfully requests that the rejection of claims 1–35 over Duluk be withdrawn.

Applicant has also found mention of a "cache" by Duluk. Specifically, Duluk states that blocks downstream of Mode Injection block 10000 (which itself is downstream of Cull block 8000, Fig. 10) "cache recently used mode information" (col. 27, ll. 11–18). This "mode information" is defined as "colors, material properties, and so on" as opposed to "spatial info" (col. 27, ll. 12–13; FIG. 10 at block 4000). Therefore, applicant respectfully notes that this teaching of cached mode information does not disclose a scratchpad containing a entry as recited in claims 1 and 27, where a value of the entry is compared to a Z value of a fragment, and the fragment is passed to a pixel pipeline based on a result of the comparing.

As noted by the Examiner, Duluk teaches that "[i]n conventional Z buffer rendering, the renderer calculates the color value ... and z value for each pixel, of each primitive, then compares the z value of the new pixel with the current Z value in the Z-buffer" (col. 20, ll. 61–64; emphasis added). Thus Duluk teaches that in such case the rendering occurs **before** the Z comparison. Applicant respectfully notes that this discussion of conventional Z buffer rendering does not teach or suggest passing a fragment to a pixel pipeline **based on** a comparison of a Z value, as recited in claims 1 and 27.

Claim 36 recites determining that a scratchpad contains an entry mapped to a pixel, determining an occlusion status of the fragment based on a value of the entry, and subsequently altering a value of the fragment. For at least the reasons set forth above, applicant respectfully submits that claim 36 and its dependent claim 37 are allowable.

Claim 38 recites a logic circuit configured to determine that a scratchpad contains an entry mapped to a pixel, to compare a Z value of the fragment to a value of the entry, and to pass the fragment to a pixel pipeline based on a result of the comparing. For at least the reasons set forth above, applicant respectfully submits that claim 38 and its dependent claims 39–44 are allowable.

Applicant respectfully submits that claims 2–26 and 28–35 are allowable at least by virtue of their dependence from claim 1 or 27. Applicant also respectfully submits that at least the following claims are also allowable for additional features recited therein:

Claim 2 (replacing a line of entries of the scratchpad according to a predetermined cache replacement policy);

Claim 11 (overwriting the value of the entry with the Z value of the fragment);

Claim 13 (determining that the entry is valid);

Claims 14, 20 (determining that the scratchpad contains a line of entries mapped to a block of pixels including the pixel);

Claim 15 (determining that the line is valid);

Claim 33 (storing the Z value of the fragment to the entry); and

Claim 34 (mapping a line of the scratchpad to a block of pixels including the pixel).

All objections and rejections having been addressed, applicant respectfully submits that the application is in condition for allowance and earnestly requests a notice to that effect. The Examiner is invited to contact the undersigned representative if the Examiner believes that any particular point or issue could be effectively addressed in such manner.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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